MINIATURE HYBRID MICROWAVE IC'S USING A NOVEL THIN-FILM TECHNOLOGY

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ABSTRACT

A novel thin-film technology for miniature hybrid microwave ICs is presented. All passive components are fully integrated on ordinary alumina ceramic substrates using the thin-film technology with very high yield. The numbers of parts and wiring processes were significantly reduced. This technology was applied to fabrication of Ku-band solid-state power amplifiers.

INTRODUCTION

Hybrid microwave integrated circuits (HMICs) were first developed in the late 60's using relatively simple technology(1). The HMICs are very useful components today for some applications to such as power devices. Most of commercially available HMICs have been constructed with chip-type passive components. In order to reduce the size, weight and cost, some approaches to integrate all passive components using thin-film technologies were reported. However, specially prepared substrates such as sapphires or ceramics with glass coating(2) were needed to improve the yield. We have developed a novel thin-film technology to fabricate thin-film capacitors and integrate them with other passive components such as thin-film resistors on ordinary alumina substrates with very high yield. Full integration of all passive components, that is, a miniature hybrid microwave IC (MHMIC), results in significant reduction of the size, number of mounting and wiring processes, and cost. A typical application is a Ku-band (14G Hz) solid-state power amplifier (SSPA).

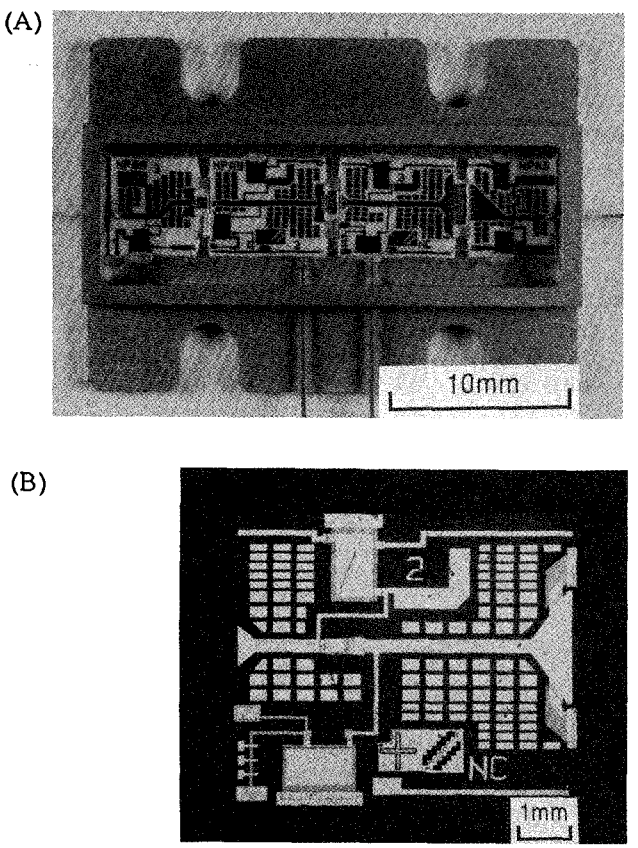

Fig.1 A solid-state power amplifier (SSPA) module constructed with miniature hybrid microwave ICs (MHMICs) fabricated by novel thin-film technology; (A) an outlook of the module, (B) a typical MHMIC including two thin-film resistors and 5 thin-film capacitors on an alumina substrate, (C) an equivalent circuit for the SSPA.

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CONSTRUCTION AND COMPARISON WITH A CONVENTIONAL HMIC

An outlook of a newly developed MHMIC for a Ku-band SSPA is shown in Fig. 1(A). It is a three-stage 1w-class power amplifier module using GaAs FET bear chips. The size of the module is 25 mm × 18 mm. Six resistors and 13 capacitors were integrated in 4 alumina substrates as shown typically in Fig.1(B). Two kinds of resistors having different thermal characteristics were integrated for canceling the temperature dependence of the GaAs FETs. Three kinds of capacitors (DC cut, matching and bypass) were integrated. An equivalent circuit for the SSPA is shown in Fig.1(C). In comparison with a conventional HMIC, the number of parts was reduced from 27(1 pacakage, 4 substrates, 3 GaAs FETs, 6 chip-type resistors and 13 chip-type capacitors) to 8 (1 package, 4 substrates and 3 GaAs FETs). The number of the wire-bondings was reduced from 28 to 15. The size was reduced by 2/3.

CERAMIC SUBSTRATES

Ordinary alumina of 99.5% were used for the substrates. As far as ceramics were used for the substrates, voids at the surface were inevitable. The size of the void was around 1 micron, even after polishing as shown in Fig.2.

The thickness of the thin-film was also around 1 micron. Therefore, the surface roughness were decisively important for the yield. To eliminate the bad effects, sapphires or ceramics with glass coating have been used so far. The newly developed process succeeded to fabricate the thin-film capacitors with very high yield on the ordinary alumina substrates having the voids.

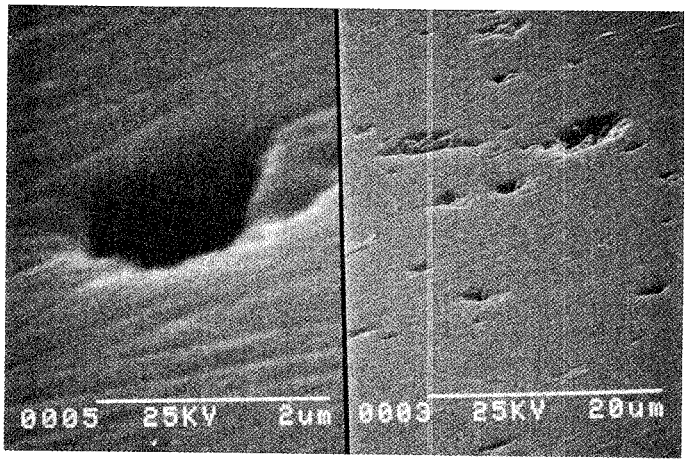

Fig.2 Typical surface structure of an ordinary alumina substrate with voids after polishing.

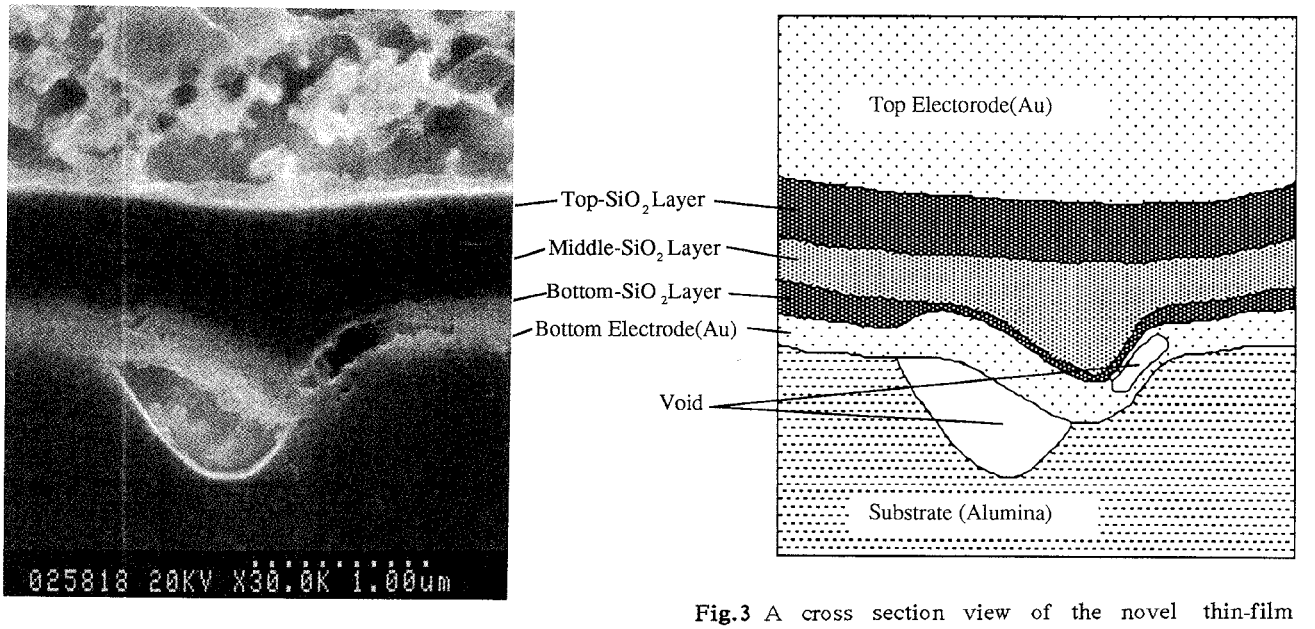

Fig.3 A cross section view of the novel thin-film capacitor composed of three-layered structure and fabricated just on a void of the substrate. As can be seen from the figure, the portion of the void is flattened by the middle SiO_2 layer.

NOVEL THIN-FILM CAPACITORS

The newly developed thin-film capacitor has a three-layered structure as shown in Fig.3. It is a cross section of the capacitor fabricated just on the void. The bottom layer is an SiO_2 film deposited by low-pressure chemical vapor deposition(LP-CVD). The middle layer is an SiO_2 film fabricated by firing spin-coated solution-state silicon oxide precursor. The top layer is an SiO_2 layer deposited by LP-CVD. The thicknesses of the layers were typically 150nm, 200 nm, and 250 nm, respectively. Using this three-layered structure, the breakdown voltage and the yield were very much improved. The breakdown voltage increased from DC15V to DC100V. The yield increased from 10% to 97%. The improvement came from the middle SiO_2 layer. As can be seen from Fig. 3, the portion of the void was flattened by the middle layer, because the layer was fabricated by spin-coating of solution-state material.The dielectric properties and the reliability of the capacitor were mainly supported by the bottom and the top SiO_2 layers deposited by LP-CVD. The Q-factor and the dielectric constant (ε_r) of the capacitor of 240 μm × 330 μm (2pF) were obtained from measuring the Q-factor and the resonant frequency of a straight line resonator with the capacitor at the center. The results are shown in Fig.4 as a function of frequency. The Q-factor depended on the thickness of the Au electrodes. When the thickness was 0.5 μm, the Q-factor was about 100 at 12 GHz, whereas when the thickness was 1 μm, it was 230. The dielectric constant was 3.6 at 12 GHz. The reliability was good enough. For example, the change of the dielectric properties after storage at 150 °C for 500 h was almost none as shown in Fig.5.

THIN-FILM RESISTORS AND FULL INTEGRATION

The resistors were tantalum nitride thin-films deposited by reactive magnetron sputtering of Ta target in Ar and nitrogen atmosphere. The temperature coefficient of the resistor was controlled by the sputtering power and the nitrogen partial pressure. Two kinds of resistors were integrated by a novel lift-off process. The resistors (R_1) connected between the voltage source for gate bias and the earth have a temperature coefficient of -1000 ppm, whereas the other resistors (R_2) have a temperature coefficient of almost 0 ppm. As a result, when the ambient temperature increases, the gate bias voltage increases, so that a decrease of gain is canceled. The typical electrical characteristics and the sputtering conditions of the resistors are summarized in Table 1. The tantalum nitride film for R_1 was very hard to etch by a conventional etchant such as a mixed solution of HF and HNO_3.

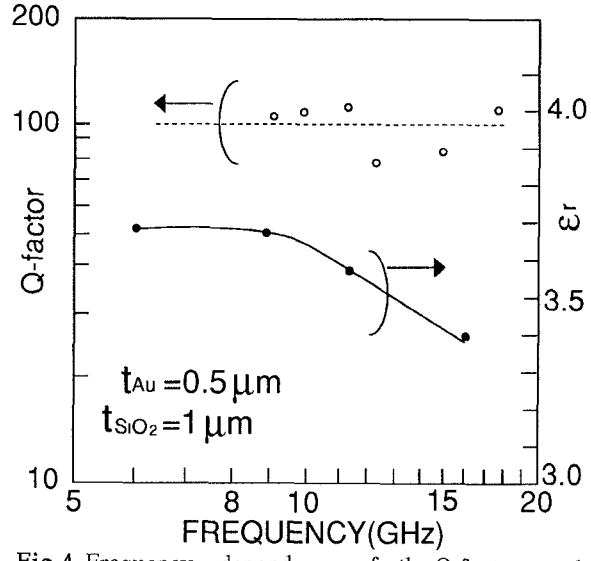

Fig.4 Frequency dependence of the Q-factor and dielectric constant of the thin-film capacitor.

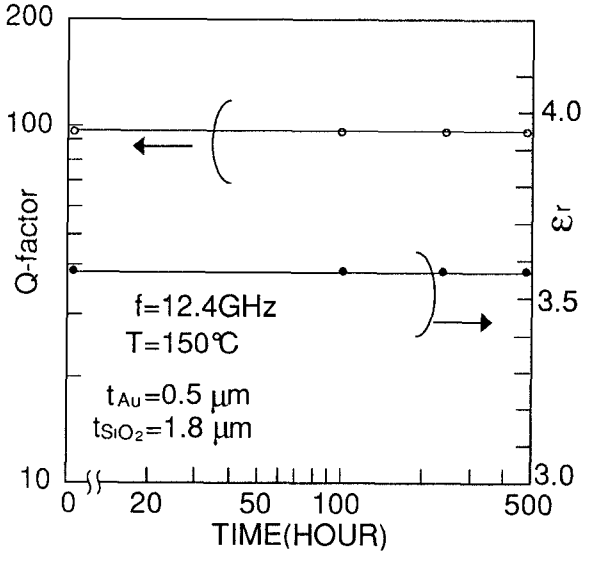

Fig.5Thermal stability of the thin-film capacitor at150°C.

Table 1 Electrical characteristics and fabrication conditions of the thin-film resistors.

	R_1	R_2
Sputtering Conditions		
Sputtering Pressure	4mmTorr	4mmTorr
N_2Partial Pressure	10 %	2.3%
RF Power	200W	400W
Substrate Temperature	300℃	300℃
Elecrical Characterristics		
Resistivity	$10^{-3}\Omega$.cm	$2x10^{-4}\Omega$.cm
Sheet Resistance	25 Ω/□	25 Ω/□
Temperature Coefficient	-1000 ppm	~0 ppm

Process Chart

1.Deposition of Lift-Off Mask (Ti;Al;Ni-Cr)
Etching of Lift-Off Mask

2.Deposition of Thin-Film Resistor-1 (TaN:400nm)
Lift-Off

3.Deposition of Thin-Film Resistor-2 (Ta_2N:80nm)
Etching of Thin-Film Resistor -2 ($HF+HNO_3$)

4.Depositiotn of Bottom Electorode (Au:1 μm)
Etching of Bottom Electorode

5.Deposititon of Bottom SiO_2 Layer (150 nm)
Etching of Bottom SiO_2 Layer

6.Spin-Coating and Firing of Middle SiO_2 Layer (200nm)

7.Deposition of Top SiO_2Layer (250 nm)
Etching ofMiddle and Top SiO_2 Layer

8.Deposition of Top Electorode (Au :2 μm)
Etching of Top Electorode and Fabricating of Microstrip Line

Fig.6 Fabrication process of the MHMIC.

Furthermore a dense etchant consisted of HF damaged the surface of the alumina substrate and deteriorated the surface roughness.
The novel lift-off process was introduced to solve this problem. Before sputtering of tantalum nitride for R_1, a lift-off mask consisted of three layered structure of Ti, Al, and Ni-Cr was fabricated. The thicknesses of the layers were 50nm, 0.5 μm, and 0.2 μm, respectively. The eaves of Ni-Cr on Al were fabricated by wet-etching. The sputtered film on this mask was easily lifted-off by wet-etching using weak etchants. The second tantalum nitride film was sputtered and etched by a weak etchant. Then the thin-film capacitors and microstrip lines were fabricated. All of the fabrication steps of the MHMIC are summarized in Fig. 6. The capacitor values and their variations of DC-cut, bypass and matching were typically 2.0pF(±3%), 30pF(±5%) and 1-5 pF(±3%), respectively.

MATCHING CIRCUITS USING THIN-FILM CAPACITORS

A key technology for impedance matching using the thin-film capacitor is grounding of the capacitor. Three methods concerning grounding, (1) 1/4 wavelength open stub, (2)via hole and (3) ribbon-bonding, as shown in Fig.7, were simulated and examined. As for the matching band-width, the second method was the best, and the first method was the worst, whereas as for the easiness of fabrication and adjustment, the second method was the worst and the third method was the best. The third method was good enough to adjust matching in a band-width of 0.5 GHz at 14GHz and very easy to fabricate. Therefore, we adopted the third method (ribbon-bonding).

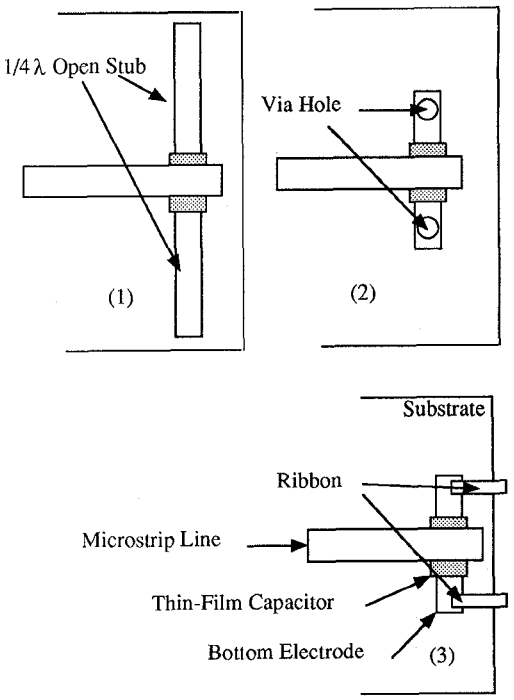

Fig.7 Grounding methods of the thin-film capacitor.

SUMMARY

The newly developed thin-film technology for the MHMIC are as follows :
(1) fabrication process of the thin-film capacitor,
(2) lift-off process for the thin-film resistor, and
(3) matching method using the thin-film capacitor.
The merits of the MHMIC are as follows:
(1) size reduction (2/3) of conventional HMIC,
(2) reduction of the number of parts (1/3),
(3) reduction of mounting and wiring processes (1/2),
(4) cost reduction due to cheap substrates and high yield, and (5) high performance due to small parasitics.

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